Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2014, Article ID 820763, 8 pages
http://dx.doi.org/10.1155/2014/820763

Hindawi

Research Article

Performance Evaluation of 14 nm FinFET-Based 6T SRAM Cell Functionality for DC and Transient Circuit Analysis

Wei Lim, Huei Chaeng Chin, Cheng Siong Lim, and Michael Loong Peng Tan

Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), 81310 Skudai, Johor, Malaysia

Correspondence should be addressed to Michael Loong Peng Tan; michael@fke.utm.my

Received 15 February 2014; Revised 28 June 2014; Accepted 6 July 2014; Published 23 July 2014

Academic Editor: Shiren Wang

As the technology node size decreases, the number of static random-access memory (SRAM) cells on a single word line increases. The coupling capacitance will increase with the increase of the load of word line, which reduces the performance of SRAM, more obvious in the SRAM signal delay and the SRAM power usage. The main purpose of this study is to investigate the stability and evaluate the power consumption of a 14 nm gate length FinFET-based 6T SRAM cell functionality for direct current (DC) and transient circuit analysis, namely, in resistor-capacitor (RC) delay. In particular, Berkeley Short-channel IGFET Model-Common Multigate (BSIM-CMG) model is utilized. The simulation of the SRAM model is carried out in HSPICE based on 14 nm process technology. A shorted-gate (SG) mode FinFET is modeled on a silicon on insulator (SOI) substrate. It is tested in terms of functionality and stability. Then, a functional SRAM is simulated with 5 GHz square wave at the input of word line (WL). Ideal square wave and square wave with 100 RC, 5 RC, 1 RC, and 0.5 RC are asserted to the WL and the bit lines (BL&BLB) of SRAM. Voltage at node q and $\overline{q}$ is observed. The simulation shows that 1 RC is the minimum square wave that will store correct value in node q and node $\overline{q}$. Thus, this discovery from the research can be used as a modeling platform for circuit designers to explore and improve the SRAM tolerance against RC delay.

1. Introduction

Static random-access memory (SRAM) constitutes a large percentage of cell area in system on chip (SOC) designs due to high number of transistors for a single SRAM cell [1]. Thus, SRAM cell typically utilizes minimum size transistor in order to realize higher density [2]. Metal-oxide-semiconductor field-effect-transistor (MOSFET) technology scaling has been used to reduce size of SRAM cell over the past three decades [3]. With the reduction of gate length that resulted in smaller SRAM cell, more SRAM cell can be allocated on the die without increasing the footprint, thus, increasing the memory storage capacity. Besides, MOSFET downscaling improves SRAM performance with higher transistor switching speed and reduces power consumption [3]. However, as the technology scaled beyond 32 nm, conventional planar MOSFETs start to fail due to the threshold voltage (V_T) variation and short channel effect (SCE) [4]. FinFET has been proven to be a better alternative for conventional nanoscale MOSFET when technology process is being scaled down below particularly at 32 nm node [5, 6]. FinFET offers several merits over MOSFET. For one, FinFET has better control over the channel due to several gates acting on the channel [7]. Because of this, FinFET has excellent electrostatic properties [8]. Besides, the FinFET's excellent gate control over the channel reduces the source-drain leakage current and suppresses the SCE. Thus, further scaling down of a FinFET is possible. Moreover, FinFET's lightly doped channel reduces random dopant fluctuation and effectively reduces the V_T variation [9]. The suppressed SCE and the enhanced gate control over channel allow the use of thicker gate oxide and, therefore, significantly reduce the gate oxide leakage current [10].

The 14 nm gate length FinFET is used as target because it will be used in the next generation of product by semiconductor manufacturing processes in a wide range of applications, namely, SRAM in this case. With each advancement in technology nodes, more SRAM cells can be positioned within a single word line (WL). For a design with many loads on a long wire, coupling capacitance can become a large factor

Table 1: Modified FinFET model parameters.

	Gate length, nm	Fins per finger
Access transistor (M5, M6)	14	2
p-FinFET (M2, M4)	14	2
n-FinFET (M1, M3)	14	4

in SRAM cell performance, namely, the rising transition of the word line and the falling transition of the local precharge signal [11]. The coupling capacitance and the resistance of WL wire introduce resistor-capacitor (RC) relay at the input signal of the WL. Besides, the wire interconnect scaling introduces a nonscaling RC, which is intolerable for a high-performance SRAM design [12]. The parasitic RC reduces the SRAM performance [13]. As a result, SRAM's RC and coupling delay correction circuit is being implemented to overcome the performance degradation [11]. Nevertheless, there has not been any work on the consequences of RC delay on SRAM output signal. It is not demonstrated how much RC delay a SRAM cell can tolerate before its functionality fails. For the first time, the FinFET-based 6T SRAM internal nodes behavior is examined by using an array of square wave input of various RC delays and the minimum RC of a functional SRAM cell is acquired.

In this paper, the stability and power evaluation of a FinFET-based 6T SRAM cell in SPICE-direct current (DC) and transient analysis are explored. Voltage transfer characteristic (VTC) of the SRAM is revealed by analyzing the SRAM retention, SRAM read, and SRAM write operation. In addition, the static noise margin (SNM) is obtained for SRAM in retention mode, access mode, and write operation. Once the SRAM is stable, transient analysis is performed in HSPICE. Following that, the RC delay is introduced to WL signal, and the value of RC delay of the input signal that causes incorrect SRAM stored node value is obtained.

2. FinFET Device Parameter

The FinFET standard model is based on the Berkeley's Berkeley Short-channel IGFET Model-Common Multigate (BSIM-CMG) SPICE library. The compact model library can be used for common multigate FETs. The FinFET default parameter is listed in the technical manual along with the Verilog-A sample model. In this exploration, a few of the parameters are modified whereas the other parameters are set as default value. The modified parameters are shown in Table 1.

In the simulation, 14 nm technology process parameters are utilized. Quantized width, which is similar to the width of a MOSFET, is utilized. Higher fins per finger means bigger width, hence stronger current flow. The equivalence width of a FinFET with single fin is the height and thickness of silicon fin that has contact with the gate. Therefore, the equivalence width of a FinFET with n fins is $n * (2 * H_{\text{fin}} + T_{\text{fin}})$ [14], where H_{fin} is fin height, while T_{fin} is fin thickness. The default values of H_{fin} and T_{fin} are 30 nm and 15 nm, respectively. Thus, the equivalence widths of M1, M2, M3, M4, M5, and M6 are 300 nm, 150 nm, 300 nm, 150 nm, 150 nm, and 150 nm, respectively.

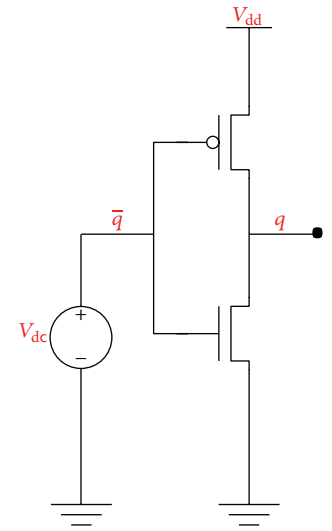

Figure 1: Schematic of single inverter.

α ratio is the write stability, while β ratio is the read stability. The access transistor and the inverter's p-FinFET have 2 fins per finger and the inverter's n-FinFET has 4 fins per finger. The α and β ratios are, therefore, 1 and 2, respectively, and are sufficient such that read disturb and write fail will not occur [15]. The V_{dd} voltage in this simulation is 1 V.

3. Inverter Model

SRAM consists of 2 inverters feeding each other in a closed loop. To analyze gain, noise margin, and power dissipation, single inverter is analyzed. Analysis of single inverter will reflect SRAM performance. Figure 1 shows the schematic for DC analysis on SRAM's inverter. DC analysis is performed at node $\overline{q}$, and voltage of node q is observed.

4. SRAM Model

A SRAM cell is constructed in HSPICE based on BSIM-CMG model card. Figure 2 shows the schematic of the SRAM cell model. $V(\text{WL})$ is word line voltage, $V(\overline{\text{BL}})$ is bit line bar voltage, and $V(\text{BL})$ is bit line voltage, while $\overline{q}$ and q are SRAM internal nodes that store 1 bit. Since the V_{dd} is 1 V, logic 1 means the voltage at node q is 1 V, whereas logic 0 means voltage at node q is 0 V. To read SRAM internal nodes value, both BL and $\overline{\text{BL}}$ are set to high. M5 and M6 are n-FinFET and are the access transistors, which serves to control the access to the SRAM internal storage during read operation and write operation. M5 and M6 will be turned on if WL is asserted. M1 and M3 are inverter's n-FinFET, while M2 and M4 are inverter's p-FinFET. Note that M4 and M3 are an inverter, M2 and M1 are another inverter. If WL is not asserted, the data in the SRAM cell is kept to a stable state, latching within the flip-flop formed by M1, M2, M3, and M4.

Table 2: Value of resistor and capacitor for different RC multipliers.

RC multiplier	Half cycle (s)	$\tau = R * C$	Resistor, Ω	Capacitor, F
100	100 ps	1 ps	1	1 p
20	100 ps	5 ps	1	5 p
1	100 ps	100 ps	1	100 p
0.5	100 ps	200 ps	1	200 p

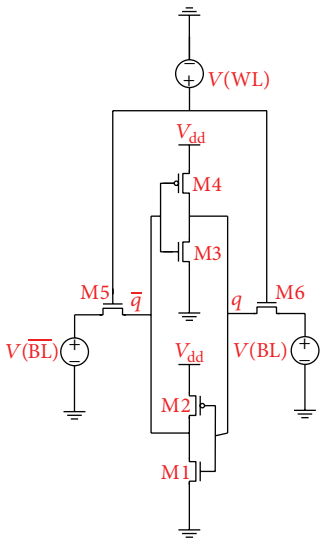

Figure 2: The schematic of single SRAM cell model.

SRAM is analyzed in terms of DC analysis and transient analysis. DC analysis of SRAM involves investigation of SRAM stability using butterfly curve. The SNM is obtained graphically, which is the side length of the maximum square that can fit inside the butterfly curve. Transient analysis of SRAM involves investigation of SRAM behavior in real time. Square wave with RC is introduced to the word line of SRAM and the changes of behavior in SRAM internal nodes is observed.

5. RC Model

After the SRAM cell is proved to be stable, square waves with 100 RC, 5 RC, 1 RC, and 0.5 RC are applied to the word line. The square wave with RC is modeled by using a resistor and a capacitor as shown in Figure 3. V_{in} is the input of perfect square wave, while $V(\mathrm{WL})$ is the square wave with RC that will be connected to WL. The input of the word line is a 5 GHz square wave. Thus, the half cycle time of the square wave is 100 ps. Table 2 shows the resistor and the capacitor value that are used to obtain different set of RC delay. A formula to calculate time constant, τ, is given by

$$\tau = \frac{\text{Half Cycles (s)}}{\text{RC multiplier}}. \quad (1)$$

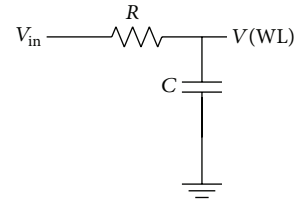

Figure 3: Resistor-capacitor circuit.

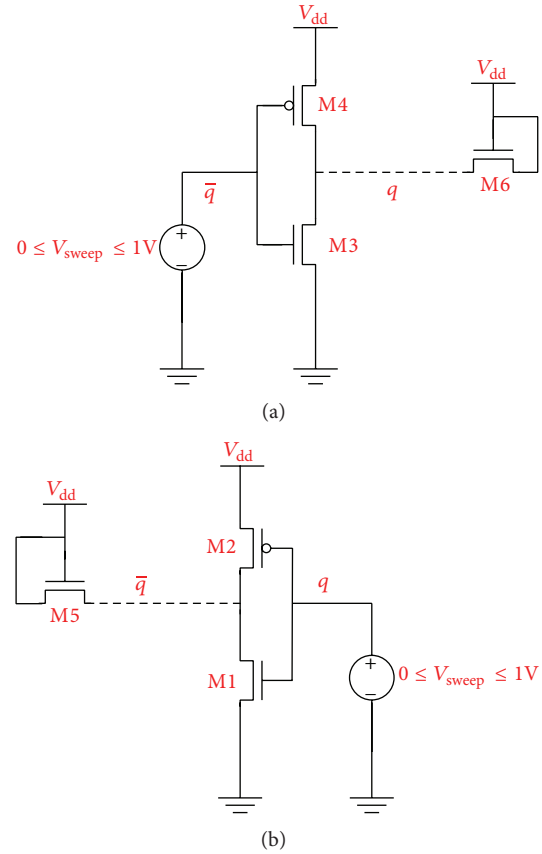

Figure 4: The schematic for butterfly curve measurement of SRAM in retention mode. The voltage source is swept between 0 to 1 V.

6. SNM Extraction

To obtain the SNM graphically, a butterfly curve is first plotted. For the measurement of the butterfly curve, the feedback of the cross-coupled inverter is separated. Then, DC analysis is performed at node q and node $\overline{q}$. The result of DC analysis is illustrated in Figure 7. Butterfly curve is obtained by toggling the X and Y axis of one of the VTC curves, and merging the two separate VTC plots together. Figures 4 and 5 show the schematic for butterfly curve measurement of SRAM in retention mode and access mode, respectively. In those figures, note that that dotted lines are not wired as originally depicted in Figure 2. Figure 6 shows the VTC measurement of SRAM in write operation. The write operation is a process of writing logic 0 to q and logic 1 to $\overline{q}$ where BL is grounded and BLB is connected to V_{dd}.

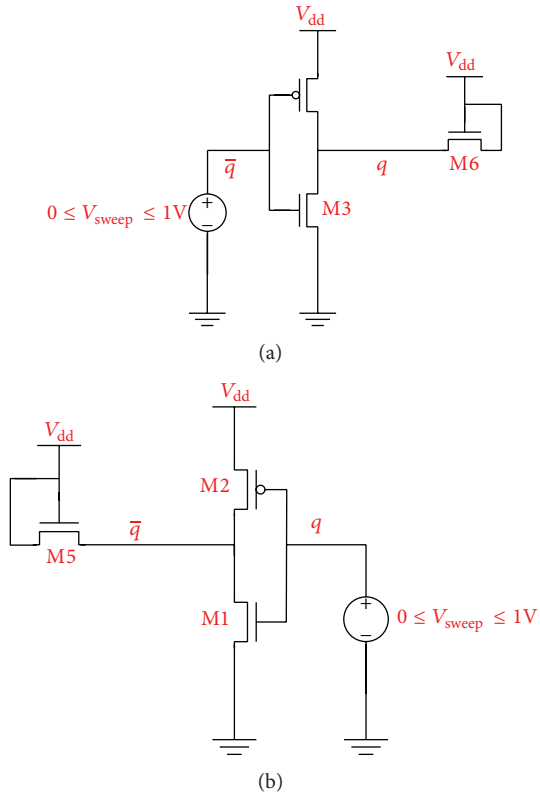

Figure 5: The schematic for butterfly curve measurement of SRAM in access mode. The voltage source is swept between 0 to 1 V.

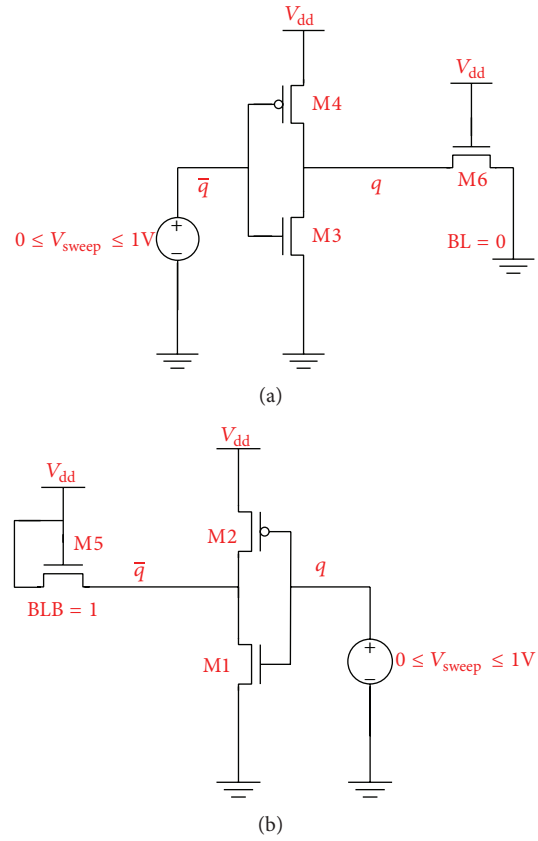

Figure 6: The schematic for butterfly curve measurement of SRAM in write operation. The voltage source is swept between 0 to 1 V.

7. Results and Discussion

Figure 7 shows the voltage transfer characteristic (VTC) of the SRAM's inverter. The pink curve is the current measured at V_{dd}, while the green curve depicts the voltage at node q. Note that the current $i(v_{dd})$ in Figure 7 is in negative for the current measurement of a p-FinFET. $V(\overline{q})$ is denoted as $V(qb)$ and vice versa.

The peak current (pointing downward) is at the point where gain of $V(q)$ is highest, that is, at $V(\overline{q}) = 0.37$ V. This is due to short circuit leakage current, where input signal causes a direct current path between V_{dd} and GND for a short period of time during switching. Thus, power dissipation is highest at this point.

By using HSPICE .measure syntax and .op syntax, the average power dissipation and static power dissipation are obtained at 12.51 mW and 2.80 mW, respectively. Thus, the dynamic power, 9.71 mW, is given by subtracting the static power dissipation from the average power dissipation. The high static power dissipation indicate weak gate control over channel as the distance between source and drain is smaller and is an issue to be tackled.

Figure 8 shows the SRAM's inverter gain (slope) and noise margin where the inverter switching threshold, noise margin, and gain of the inverter are measured. Inverter switching threshold, (V_m) is the intersection of VTC curve $V(q)$ with the linear curve of $V(q) = V(qb)$. From Figure 8, V_m is calculated at 0.37 V. V_m is not centered at 0.5 V, but slightly to the left. This indicated a strong n-FinFET and a weak p-FinFET configuration. This is an expected condition for any SRAM with acceptable α and β ratio.

Noise margin is the performance metric of an inverter of how much it can tolerate noise or unwanted signal. Input low voltage, V_{IL}, and input high voltage, V_{IH}, are obtained when the slope of the VTC curve is −1. Any voltage lower than V_{IL} will be logic 0, whereas any voltage higher than V_{IH} will be logic 1. From Figure 8, V_{IL} is 0.19 V and V_{IH} is 0.43 V. Thus, the noise margin high (NMH) is given as 1 V − 0.43 V = 0.57 V, while noise margin low (NML) is given as 0.19 V − 0 V = 0.19 V. A high gain is desired for fast switching speed (low delay) and low leakage current. The gain of the inverter is calculated to be 7.60 from the intersection of VTC at V_m.

Figures 9, 10, and 11 show the butterfly curve of SRAM in retention mode, access mode, and write operation, respectively. SNM is obtained graphically from the butterfly curve. The SNM of SRAM in retention mode and access mode are 0.24 V and 0.12 V, respectively. Endo et al. [16] obtained SNM of 0.19 V for SRAM in retention mode with 0.3 V and 0.36 V gate voltage on independent-gate (IG) mode FinFET. In our work, the SNM of a SRAM in write operation is at 0.38 V. This value is consistent with the findings of Endo et al. [16] where they obtained SNM of 0.35 V for SRAM in write operation. Higher SNM is expected for SG-FinFET [17].

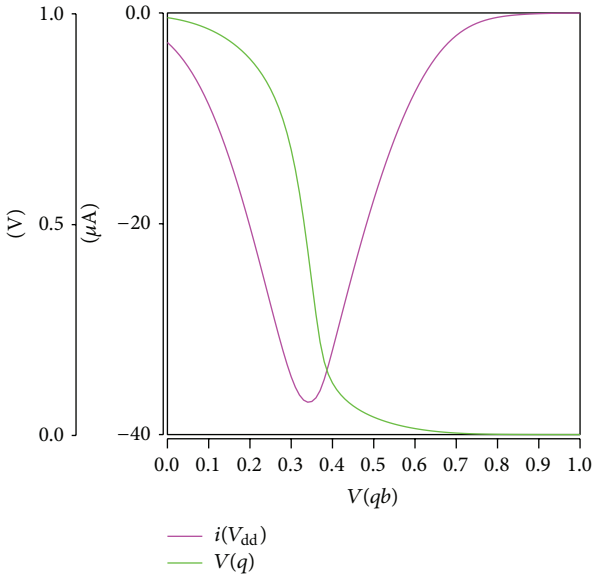

Figure 7: VTC curve and current of single inverter.

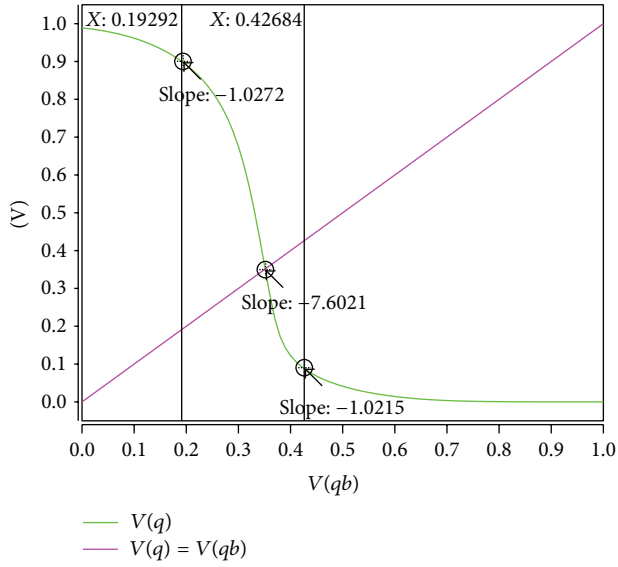

Figure 8: Inverter slope and noise margin.

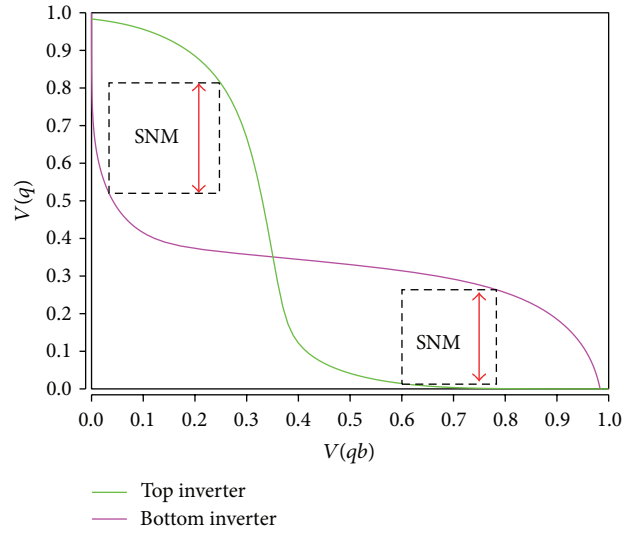

Figure 9: The butterfly curve of SRAM in retention mode.

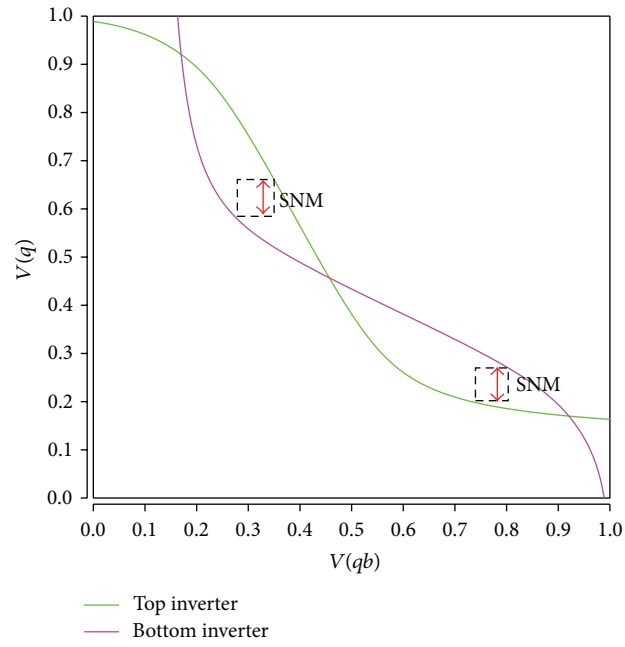

Figure 10: The butterfly curve of SRAM in access mode.

Once SRAM cell is stable, a transient analysis is performed in HSPICE. Figure 12 shows the SRAM transient analysis over 800 ps, with input of an ideal square wave voltage without any RC delay. However, in the nonideal case, RC delay builds up at the input voltage of WL and affects the overall SRAM performance.

Four operations are performed during the 800 ps cycle. Each operation is executed when WL is asserted, which is at the increment of V(WL) at 100 ps, 300 ps, 500 ps, and 700 ps. At 0 ps to 100 ps, node q is initialized to logic 1. The data in SRAM cell held in latch. At the first assertion of WL, zero is written into SRAM cell. To store logic 0 into the SRAM cell, V(BL) is set to zero. Correct sizing of SRAM ensures the data in latch is overwritten. At the second assertion of WL, a read operation is performed. During the read operation, both bit lines are precharged to a logical 1, and, then, WL is asserted. At the third assertion of WL, one is written into SRAM cell, and, at the forth assertion of WL, a read operation is performed.

Figure 13 shows the extraction of the top inverters from Figure 2. The slight increment of voltage at node q from 300 ps to 400 ps and at node $\overline{q}$ from 700 ps to 800 ps is due to pull up by V_{dd} through the access transistors, which are M5 and M6 in Figure 2. From 300 ps to 400 ps, $\overline{q}$ is 1 V. Therefore, M4 is cut-off and it is not shown in Figure 13. On the other hand, M3 and M6 are active. They can be rearranged in simpler vertical form.

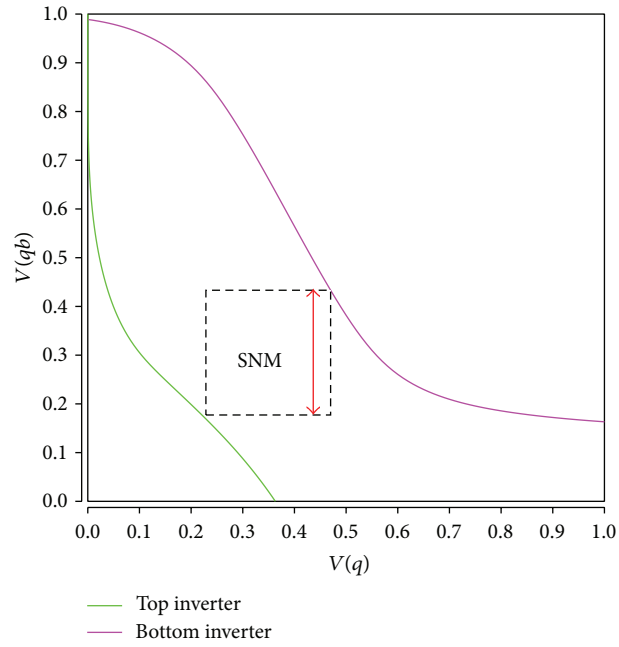

Figure 11: The VTC curve of SRAM in write operation.

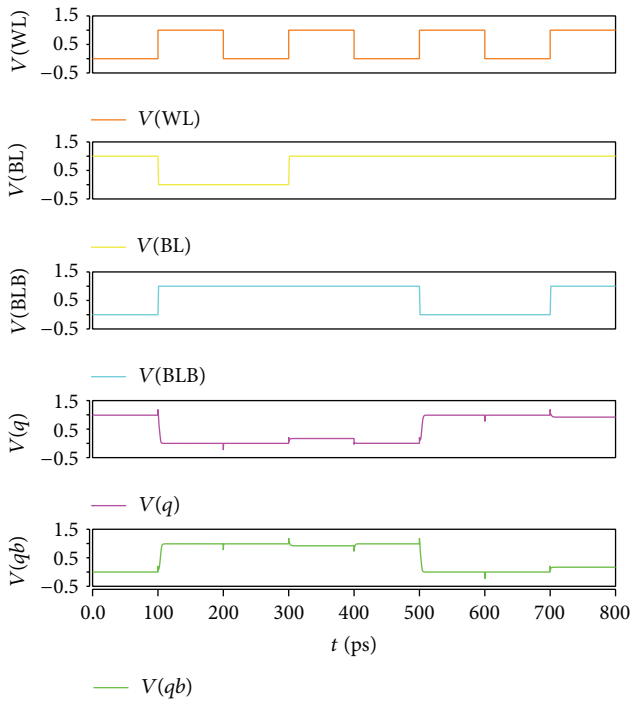

Figure 12: SRAM transient analysis over 800 ps.

The transistor sizing of M3 is larger than that of a M6 due to a high β ratio, thus, giving M3 a lower resistance compared to M6. Based on the voltage divider rule, node q yields a lower voltage. As long as the width of M3 > M6, node q will not be higher than 0.5 V when $\overline{q} = 1$ V. This is important to avoid the transistor from inverting and causing a read disturb.

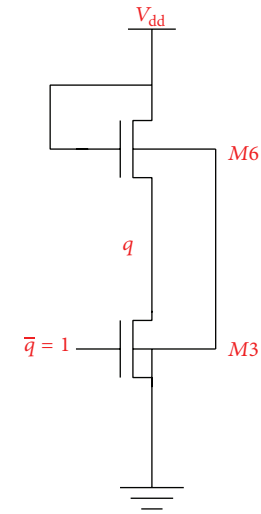

Figure 13: Extraction of M3 and M6 from Figure 2.

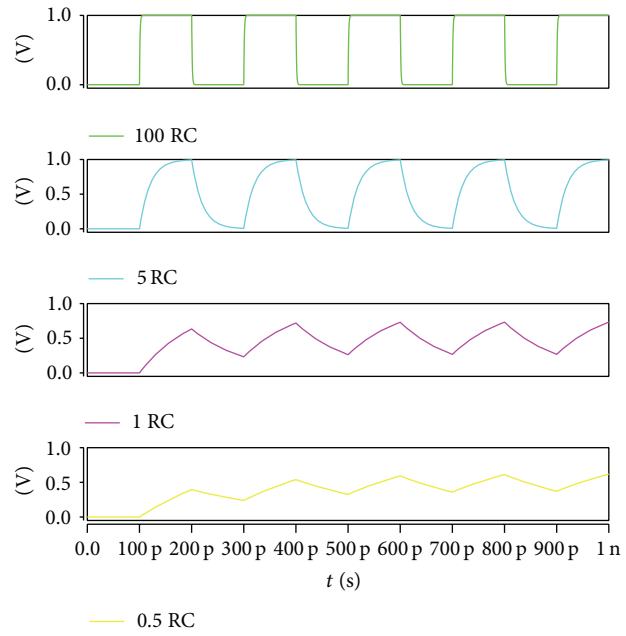

Figure 14: Periodic wave input with different RC delay.

Figure 14 illustrates the periodic wave input with different RC delay. By definition, 5 RC is the minimum RC that will complete the charge and the discharge process, producing full rail-to-rail swing. The square wave input is applied to word line, and the transient analysis in Figure 8 is performed to yield the output shown in Figure 15.

Figure 15 depicts the SRAM transient analysis within 800 ps for periodic wave input of 100 RC, 5 RC, 1 RC, and 0.5 RC word line voltages. The result in Figure 15 is separated into 8 sections and is analyzed separately. In Section 1, the SRAM cell is initialized to store 1. In Section 2, WL is asserted, and the SRAM internal nodes are influenced by V(BL) and V(BLB). For V(WL) with 100 RC, $V(q)$ drops to

Table 3: Comparison of metric performance and power consumption of word line for a wide range of various RCs. The number in brackets shows the percentage of increase over the parameter shown for 100 RC.

Metric performance	100 RC	5 RC	1 RC
Time delay, s	3.17×10^{-12}	1.01×10^{-11} (+218.61%)	2.57×10^{-11} (+710.73%)
Average power, W	2.58×10^{-3}	2.63×10^{-02} (+919.38%)	9.29×10^{-02} (+3500.78%)
Power-delay product (PDP)	8.18×10^{-15}	2.65×10^{-13} (+3139.61%)	2.39×10^{-12} (+29117.60%)
Energy-delay product (EDP)	2.59×10^{-26}	2.67×10^{-24} (+10208.88%)	6.12×10^{-23} (+236193.44%)

0 instantaneously. For V(WL) with lower RC, node q voltage drop is more gradual.

V(WL) decreases in Section 3 and the peak voltage is obtained at the end of Section 2 at 200 ps. At 200 ps, V(WL) of 0.5 RC peaks at 0.4 V, and it is less than V_{IH}, which is 0.43 V from Figure 8. It is still not considered as logical 1. Thus, the drain current through access transistor is not strong enough to flip the signal at nodes q and $\overline{q}$. As a result, the SRAM is unable to store 0 at 200 ps. In Section 3, V(WL) of 0.5 RC is decreasing, and the signal at node q is gradually stabilizing at 1. Nevertheless, note that SRAM is storing the incorrect value for V(WL) of 0.5 RC at $V(q)$ and $V(qb)$. In Section 4, SRAM is in read operation. V(WL) of 0.5 RC increases from 0.3 V to 0.5 V, but since both V(BL) and V(BLB) are high, $V(q)$ and $V(qb)$ remain unchanged and incorrect values are read. In Section 5, V(WL) of 0.5 RC slowly decay and node q is unchanged. In Section 6, 1 is written into SRAM cell. For V(WL) of 100 RC, 5 RC, and 1 RC, the write operation is successful, with noticeable and longer delay for lower RC. Nevertheless, the voltage at node q linger at 1 for V(WL) of 0.5 RC. In Section 7, the SRAM internal nodes are consistent for all V(WL). In Section 8, SRAM is in read operation and no significant change is observed for the SRAM internal nodes.

Table 3 shows the comparison of time delay, average power, power-delay product (PDP), and energy-delay product (EDP) for different RC input square wave at SRAM's word line. Both performance and power consumption deteriorate with RC delay. As such, square wave with a high RC delay is desirable to improve performance and reduce power consumption.

8. Conclusions

FinFET is a promising substitute for MOSFET to remove the challenge and obstacle faced by conventional MOSFET beyond 32 nm technology nodes. The use of FinFET has enabled further scaling of SRAM due to steeper subthreshold slope, reduced random dopant fluctuation, and relief of high-K material as gate oxide. However, as technology node decreases, parasitic RC is an issue to be concerned in SRAM design due to SRAM coupling capacitance and wire scaling. RC delay is an undesired yet unavoidable problem. From this work on 14 nm FinFET, it is revealed that 1 RC is the

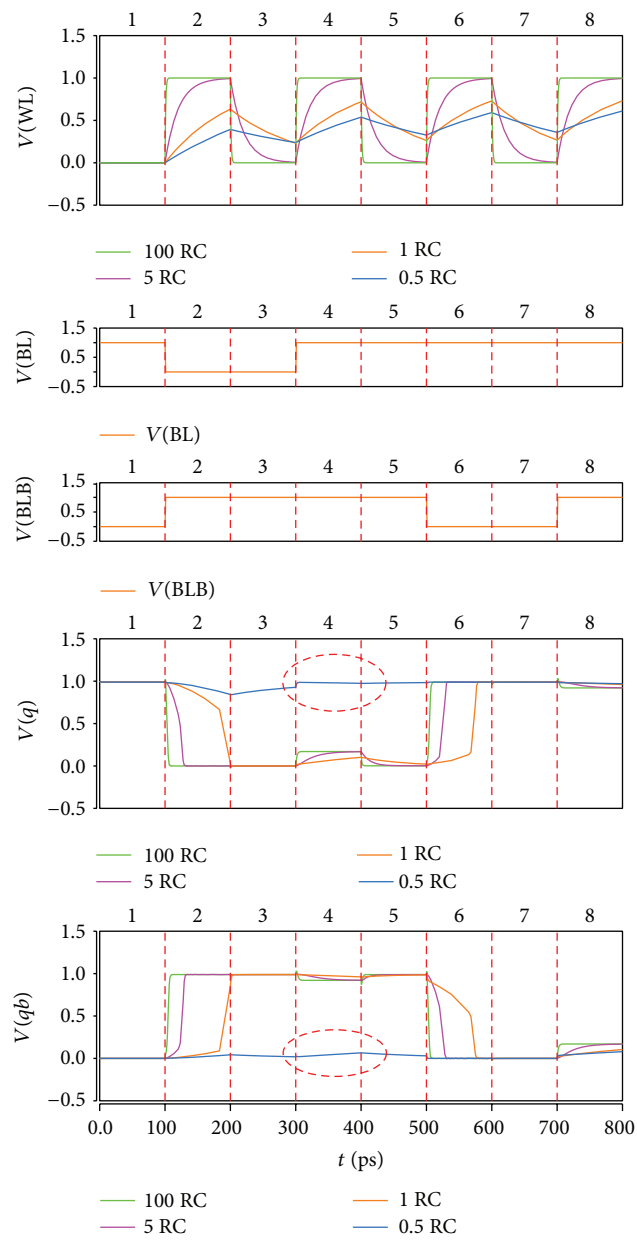

Figure 15: SRAM transient analysis within 800 ps for periodic wave input of 100 RC, 5 RC, 1 RC, and 0.5 RC word line voltages.

maximum tolerance for a SRAM cell to function correctly based on the SRAM metric performance for a wide range of various RCs, namely, time delay, average power, PDP, and EDP. This discovery can serve as a reference for SRAM circuit designers to understand the consequences in terms of RC delay when they are scaling down the SRAM cell. Circuit testers can benefit from the simulation results by comparing the simulation result with their device under test (DUT) to observe the severity of RC delay.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to thank the Research Management Centre (RMC) of Universiti Teknologi Malaysia (UTM) for providing a tremendous support conduciveness to the research environment needed to complete project of this magnitude with personnel of far-reaching background. The authors would like to acknowledge the financial support from UTM GUP Research Grant (Vote nos. Q.J130000.2523.05H64 and Q.J130000.2523.05H59) and Fundamental Research Grant Scheme (FRGS) (Vote nos. R.J130000.7823.4F247 and R.J130000.7823.4F314) of the Ministry of Higher Education (MOHE), Malaysia.

References

[1] A. S. Pavlov, *Design and test of embedded SRAMs [Ph.D. thesis]*, University of Waterloo, Waterloo, Canada, 2005.

[2] V. Sharma, *SRAM Bit Cell Optimization*, Springer Science, Business Media, New York, NY, USA, 2013.

[3] H. Iwai, "Roadmap for 22 nm and beyond (invited paper)," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1520–1528, 2009.

[4] H. Kawasaki, V. S. Basker, T. Yamashita et al., "Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond," in *Proceedings of the International Electron Devices Meeting (IEDM '09)*, pp. 1–4, December 2009.

[5] F. Wang, Y. Xie, K. Bernstein, and Y. Luo, "Dependability analysis of nano-scale FinFET circuits," in *Proceedings of the IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*, pp. 399–404, Karlsruhe, Germany, March 2006.

[6] B. Swahn and S. Hassoun, "Gate sizing: FinFETs vs 32nm bulk MOSFETs," in *Proceedings of the 43rd Design Automation Conference*, pp. 528–531, 2006.

[7] T. Poiroux, M. Vinet, O. Faynot et al., "Multiple gate devices: advantages and challenges," *Microelectronic Engineering*, vol. 80, pp. 378–385, 2005.

[8] R. Jatooth, M. Veshala, and K. R. Reddy, "Reduction of short-channel effects in FinFET," *International Journal of Engineering and Innovative Technology*, vol. 2, no. 9, 2013.

[9] A. B. S. Y. Kobayashi, K. Tsutsui, K. Kakushima, P. Ahmet, V. R. Rao, and H. Iwai, "Analysis of threshold voltage variations of FinFETs relating to short channel effects," *ECS Transactions*, vol. 16, no. 40, pp. 23–27, 2009.

[10] S. A. Tawfik, Z. Y. Liu, and V. Kursun, "Independent-gate and tied-gate FinFET SRAM circuits: design guidelines for reduced area and enhanced stability," in *Proceedings of the International Conference on Microelectronics*, pp. 370–373, 2007.

[11] D. G. Behrends, T. A. Christensen, T. R. Hebig, M. Launsbach, and D. M. Nelson, "Implementing rc and coupling delay correction for sram," USA Patent, 2013.

[12] J. Warnock, "Circuit and PD challenges at the 14 nm technology node," in *Proceedings of the ACM International Symposium on Physical Design (ISPD '13)*, pp. 66–67, March 2013.

[13] F. Nemati and J. D. Plummer, "Novel thyristor-based SRAM cell (T-RAM) for high-speed, low-voltage, giga-scale memories," in *Proceedings of the IEEE International Devices Meeting, Technical Digest (IEDM '99)*, pp. 283–286, Washington, DC, USA, December 1999.

[14] R. Ramesh, M. Madheswaran, and K. Kannan, "Optical effects on the characteristics of a nanoscale FinFET," *Progress In Electromagnetics Research B*, no. 21, pp. 235–255, 2010.

[15] R. D. Adams, *High Performance Memory Testing: Design Principles, Fault Modeling and Self-Test*, Springer, Boston, Mass, USA, 2003.

[16] K. Endo, S. O'Uchi, T. Matsukawa et al., "Enhancing SRAM performance by advanced FinFET device and circuit technology collaboration for 14nm node and beyond," in *Proceedings of the Symposium on VLSI Technology Digest of Technical Papers (VLSIT '13)*, pp. T214–T215, June 2013.

[17] A. Muttreja, N. Agarwal, and N. K. Jha, "CMOS logic design with independent-gate FinFETs," in *Proceedings of the 25th IEEE International Conference on Computer Design (ICCD '07)*, vol. 1, pp. 560–567, Lake Tahoe, Calif, USA, October 2007.